High-κ/Metal–Gate Stack and Its MOSFET Characteristics

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***Abstract*—We show experimental evidence of surface phonon scattering in the high-κ dielectric being the primary cause of channel electron mobility degradation. Next, we show that midgap TiN metal–gate electrode is effective in screening phonon scattering in the high-κ dielectric from coupling to the channel under inversion conditions, resulting in improved channel electron mobility. We then show that other metal–gate electrodes, such as the ones with n+ and p+ work functions, are also effective in improving channel mobilities to close to those of the conventional SiO_2/poly-Si stack. Finally, we demonstrate this mobility degradation recovery translates directly into high drive performance on high-κ/metal–gate CMOS transistors with desirable threshold voltages.**

***Index Terms*—Atomic layer deposition (ALD), CMOS transistors, Hafnium Oxide (HfO2), high-κ dielectric, metal–gate electrode, remote phonons.**

I. Introduction

THE SILICON industry has been scaling silicon dioxide (SiO_2) aggressively for the past 15 years for low-power, high-performance CMOS transistor applications. Recently, SiO_2 with physical thickness of 1.2 nm has been implemented in the 90-nm logic technology node [1]. In addition, research transistors with 0.8-nm (physical thickness) SiO_2 have been demonstrated in the laboratory [2], [3]. However, continual gate oxide scaling will require high-κ gate dielectric (κ being the dielectric constant) since the gate oxide leakage in SiO_2 is increasing with reducing physical thickness and SiO_2 will eventually run out of atoms for further scaling. The majority of the high-κ gate dielectrics investigated are Hf-based and Zr-based [4]–[6]. Both poly-Si and metals are being evaluated as the gate electrodes for the high-κ gate dielectrics [7], [8].

There are many challenges reported in literature in replacing SiO_2 with high-κ dielectrics for high-performance CMOS applications [9]–[11]. It has been reported that Fermi-level pinning at the high-κ/poly-Si transistors causes high threshold voltages in MOSFET transistors [9], resulting in poor transistor drive performance. It has also been reported that high-κ/poly-Si transistors exhibit severely degraded channel mobility [12], [13]. A proposed model is that the mobility degradation is due to the coupling of low-energy surface optical (SO) phonon modes arising from the polarization of the high-κ dielectric to the inversion channel charge carriers [14], and that metal–gate may be more effective in screening the high-κ's SO phonons from coupling to the channel under inversion conditions [14], [15]. On the other hand, metal–gate electrodes with the correct work functions are required for high-performance CMOS logic applications on bulk Si [16].

To understand the various physical scattering mechanisms that limit channel electron mobility in the high-κ dielectric, we experimentally measure the effective inversion electron mobility as a function of temperature and transverse electric field (E_{eff}) in the HfO_2/poly-Si stack, and conclude that surface phonon scattering is the primary cause of electron mobility degradation in the HfO_2. We then show that the use of midgap TiN metal–gate electrode is effective in screening the remote phonon electron interaction and improves the channel electron mobility. In addition, we show that this is generally true of other metal–gate electrode materials system with n+ and p+ work functions, and that the expected high drive current performance for both the n-channel and p-channel MOSFET's with the desirable threshold voltages is indeed obtained.

II. Mobility Measurements and Discussion

In this letter, atomic layer deposition (ALD) HfO_2 is used as an example of high-κ gate dielectric for the study. Physical vapor deposition (PVD) TiN metal is deposited using a dc magnetron reactive sputtering process off a titanium target in nitrogen ambient to form the gate electrode. The flatband voltages of the HfO_2/poly-Si and HfO_2/TiN (midgap) stacks plotted against electrical oxide thickness show similar slopes as the standard SiO_2/poly-Si stack, suggesting that the amount of fixed charge present in the HfO_2 is similar to that in the standard SiO_2[15]. In addition, the subthreshold slopes of the long-channel high-κ transistors are normal, suggesting that the amount of interface traps present is minimal [15]. The effective electron mobilities (μ_{eff}) of the HfO_2/poly-Si and SiO_2/poly-Si stacks are measured as a function of temperature and transverse electric field (E_{eff}). Fig. 1 compares the temperature sensitivity factor, i.e., the rate of change of the reciprocal of μ_{eff} with respective to temperature (T) or $[d(1/\mu_{\text{eff}})/\text{dT}]$, of the high-$\kappa$/poly-Si stack to that of the SiO_2/poly-Si stack versus E_{eff}. In the case where coulombic scattering is dominant, the net value of this temperature sensitivity factor will be negative. In the case where phonon scattering is dominant, the net value of this factor will be positive. The results show that in the E_{eff} range of 0.5 to 1.2 MV/cm, the value of $[d(1/\mu_{\text{eff}})/\text{dT}]$ is positive for both the high-κ/poly-Si and SiO_2/poly-Si stacks, indicating that phonon scattering is important in both cases. However, the value of $[d(1/\mu_{\text{eff}})/\text{dT}]$ of the high-κ dielectric is

Manuscript received February 26, 2004; revised March 18, 2004. The review of this letter was arranged by Editor B. Yu.

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Digital Object Identifier 10.1109/LED.2004.828570

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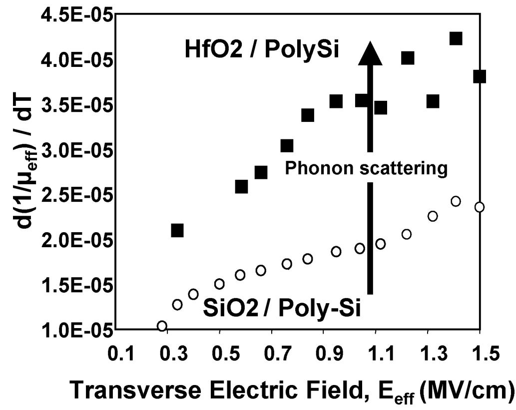

Fig. 1. Experimental evidence of phonon scattering in the high-κ dielectric. The net value of the temperature (T) sensitivity factor, $[d(1/\mu_{\mathrm{eff}})/\mathrm{d}T]$, is negative when coulombic scattering dominates and positive when phonon scattering dominates.

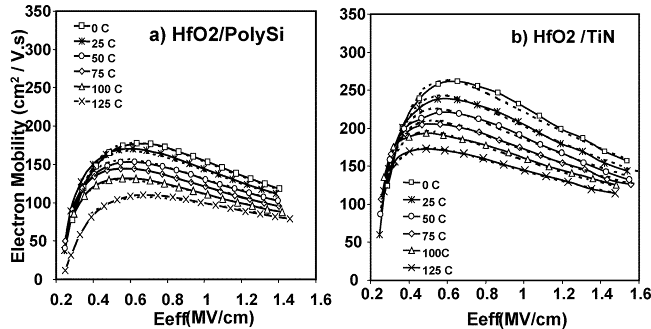

Fig. 2. Experimental (symbols) and fitted data based on physical models (dashed line) as a function of temperature and E_{eff} for (a) HfO_2/poly-Si and (b) HfO_2/TiN gate stacks.

higher than that of the SiO_2, suggesting that phonon scattering is more severe in the former. To quantify the degradation of mobility due to surface phonon scattering alone, full inverse modeling is performed based on the mobility measurement data. Fig. 2 shows the measured electron channel mobilities for HfO_2/poly-Si and HfO_2/TiN gate stacks as a function of temperature (0 °C to 125 °C) and E_{eff}, and the excellent fits to the target data-sets. Because of their similar dependence on temperature and E_{eff}, remote surface optical phonons and surface acoustic phonons were treated synonymously as surface phonons. Fig. 3 compares the surface phonon limited mobility of the HfO_2/poly-Si and HfO_2/TiN stacks to that of the standard SiO_2/poly-Si stack versus E_{eff} at 25 °C. The data shows that the HfO_2/poly-Si stack has significant mobility degradation compared to the SiO_2/poly-Si stack due to the surface phonon scattering. The data also shows that the use of midgap TiN metal–gate electrode significantly improves the high-κ mobility, suggesting that the midgap TiN (with higher free electron density) gate effectively screens and reduces the surface phonons from coupling to the inversion channel, whereas depleted poly-Si gate (with lower free electron concentration) is less effective. The screening mechanism is very similar to the commonly reported reduction in interface optical phonon scattering strengths observed in metal polar semiconductor systems [17].

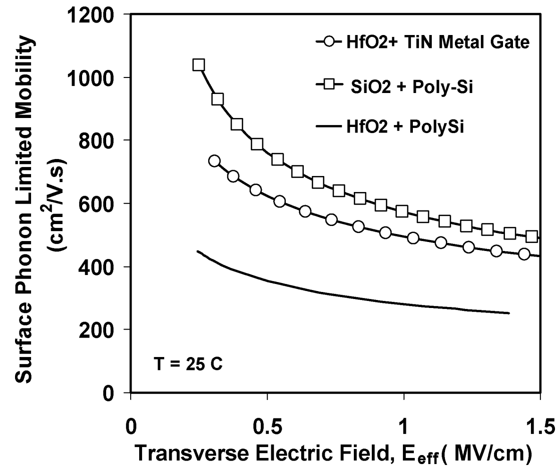

Fig. 3. Surface phonon limited mobility component at room temperature extracted from the fitted data using inverse modeling technique. The use of midgap TiN metal gate significantly improves channel mobility in the high-κ gate dielectric compared to the conventional poly-Si gate.

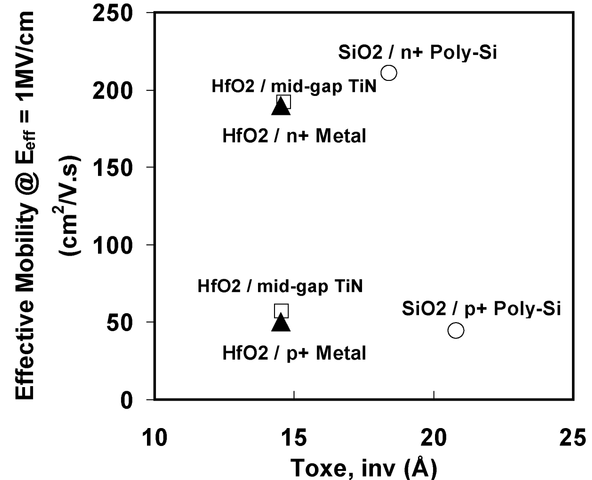

Fig. 4. Use of metal–gate electrodes with n+ and p+ work functions improves the n-channel and p-channel room temperature mobilities respectively in the high-κ dielectric (HfO_2) to close to those of the conventional $Si0_2$/poly-Si stack like midgap TiN electrode.

III. MOSFET CHARACTERISTICS

The measurement and modeling data show that the use of a midgap metal–gate electrode such as PVD TiN effectively screens the surface phonons and improves the channel mobility. In general, this is true in any metal–gate/high-κ/semiconductor system, irrespective of the work function of the metal. Fig. 4 shows that other metals, such as the ones with n+ and p+ work functions, can also improve the n-channel and p-channel mobilities at room temperature, respectively, to close to those of the standard SiO_2/poly-Si stack. The n+ and p+ metal–gate electrodes used in this study have work functions that are within 100 mV from those of the standard n+ and p+ poly-Si gate electrodes on SiO_2. We have successfully fabricated high-κ/metal–gate CMOS transistors with 80-nm physical gate length using the metal–gate electrodes with n+ and p+ work functions. The resulting transistors have 1.0-nm equivalent oxide thickness and electrical oxide thickness of 1.45 nm

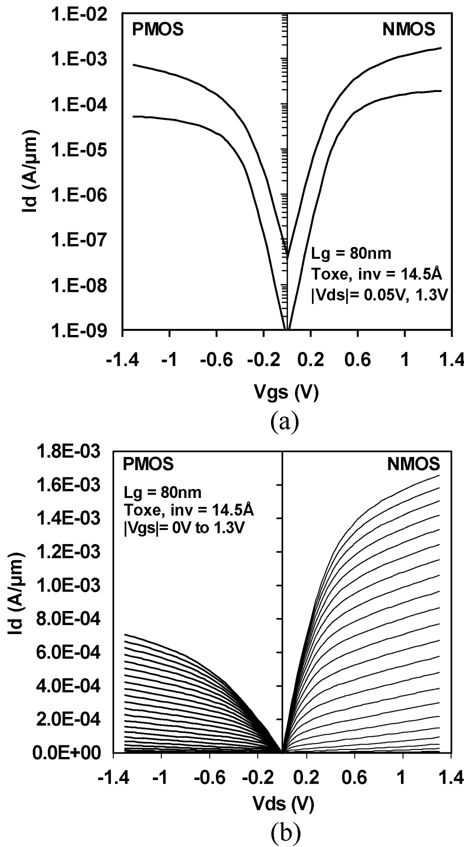

Fig. 5. (a) I_d–$V_{\rm gs}$ and (b) I_d–$V_{\rm ds}$ characteristics of the n-channel and p-channel high-κ/metal–gate MOSFETs.

at inversion. The subthreshold I_d–$V_{\rm gs}$ and family of I_d–$V_{\rm ds}$ characteristics of the n-channel and p-channel MOSFET's are shown in Fig. 5(a) and (b), respectively. The n-channel high-κ/metal–gate MOSFET has $I_{\rm on} = 1.66$ mA/um and $I_{\rm off} = 37$ nA/um, while the p-channel high-κ/metal–gate MOSFET has $I_{\rm on} = 0.71$ mA/um and $I_{\rm off} = 45$ nA/um at $V_{\rm ds} = 1.3$ V. The very high drive currents are expected because of the reduction in inversion electrical gate oxide thickness and, hence, the increase in channel inversion charge.

IV. Summary

In this brief, we showed experimental evidence that surface phonon scattering in the high-κ dielectric is the primary cause of channel electron mobility degradation and that the use of a midgap TiN metal–gate electrode is effective in screening phonon scattering in the high-κ dielectric from coupling to the channel under inversion conditions, resulting in improved channel electron mobility. We also showed that other metal–gate electrodes, such as the ones with n+ and p+ work functions, are equally effective in improving channel mobilities to close to those of the conventional SiO_2/poly-Si stack. Finally, we showed that high-κ/metal–gate CMOS transistors with the expected high drive currents can be experimentally achieved by using metal–gate electrodes with n+ and p+ work functions 1) to provide the right threshold voltages and 2) to improve the channel mobilities for both the n-channel and p-channel MOSFETs. The improvement in drive currents is due to the scaling of inversion electrical gate oxide thickness and increase in channel inversion charge. We believe that this is a very important exercise because it shows that very high-performance high-κ CMOS transistors can be experimentally achieved with the use of metal–gate electrodes on high-κ gate dielectric.

References

[1] S. Thompson *et al.*, "A 90-nm logic technology featuring 50-nm strained silicon channel transistors, 7 layers of Cu interconnects, low-κ ILD, and 1 μm^2 SRAM cell," in *IEDM Tech. Dig.*, 2002, pp. 61–64.

[2] R. Chau *et al.*, "30 nm physical gate length CMOS transistors with 1.0 ps n-MOS and 1.7 ps p-MOS gate delays," in *IEDM Tech. Dig.*, 2000, pp. 45–48.

[3] ——, "Silicon nano-transistors for logic applications," *Phys. E, Low-Dimensional Syst. Nanostructures*, vol. 19, no. 1–2, pp. 1–5, 2003.

[4] R. Choi *et al.*, "Fabrication of high quality ultra-thin HfO_2 gate dielectric MOSFET's using deuterium anneal," in *IEDM Tech. Dig.*, 2002, pp. 613–616.

[5] G. Lucovsky, B. Rayner, Y. Zhang, and J. Whitten, "Experimental determination of band offset energies between Zr silicate alloy dielectrics and crystalline Si substrates by XAS, XPS and AES and *ab initio* theory: A new approach to the compositional dependence of direct tunneling currents," in *IEDM Tech. Dig.*, 2002, pp. 617–620.

[6] S. Inumiya *et al.*, "Fabrication of HfSiON gate dielectrics by plasma oxidation and nitridation, optimized for 65 nm node low power CMOS applications," in *Symp.VLSI Tech. Dig.*, Kyoto, Japan, 2003, pp. 17–18.

[7] Y. Kim *et al.*, "Conventional poly-Si gate MOS-transistors with a novel, ultrathin Hf-oxide layer," in *Symp. VLSI Tech. Dig.*, Kyoto, Japan, 2003, pp. 167–168.

[8] S. B. Samavedam *et al.*, "Dual-metal gate CMOS with HfO_2 gate dielectric," in *IEDM Tech. Dig.*, 2003, pp. 433–436.

[9] C. Hobbs *et al.*, "Fermi level pinning at the poly-Si/metal oxide interface," in *Symp. VLSI Tech. Dig.*, Kyoto, Japan, 2003, pp. 9–10.

[10] R. M. Wallace and G. Wilk, "High-κ gate dielectric materials," *MRS Bull.*, vol. 27, no. 3, pp. 192–197, 2002.

[11] V. Mistra, G. Lucovsky, and G. Parsons, "Issues in high-κ gate stack interfaces," *MRS Bull.*, vol. 27, no. 3, pp. 212–216, 2002.

[12] E. P. Gusev *et al.*, "Ultrathin high-κ gate stacks for advanced CMOS devices," in *IEDM Tech. Dig.*, 2001, pp. 451–454.

[13] J. Lee *et al.*, "High-κ dielectrics and MOSFET characteristics," in *IEDM Tech. Dig.*, 2003, pp. 95–98.

[14] M. Fischetti, D. A. Neumayer, and E. A. Cartier, "Effective electron mobility in Si inversion layers in metal–oxide-semiconductor systems with a high-κ insulator: the role of remote phonon scattering," *J. Appl. Phys.*, vol. 90, p. 4587, 2001.

[15] S. Datta *et al.*, "High mobility Si/SiGe strained channel MOS transistors with HfO_2/TiN gate stack," in *IEDM Tech. Dig.*, 2003, pp. 653–656.

[16] Q. Lu, Y. C. Yeo, P. Ranade, H. Takeuchi, T.-J. King, C. Hu, S. C. Song, H. F. Luan, and D.-L. Kwong, "Dual-metal gate technology for deep-submicron CMOS transistors," in *Symp. VLSI Tech. Dig.*, 2000, pp. 72–73.

[17] A. R. Bhatt *et al.*, "Reduction of interface phonon modes using metal–semiconductor heterostructures," *J. Appl. Phys.*, vol. 73, pp. 2338–2342, 1993.